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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,890	FITZGERALD, EUGENE A.	
	Examiner	Art Unit	
	DUNG A. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment dated 3/2/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *80-84,87 and 88* is/are allowed.

6)☒ Claim(s) *32-70* is/are rejected.

7)☒ Claim(s) *71-76* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/2/07;3/2/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DLe

Set of claims 32- 38, 40- 47, 53-54, 65-66, 77-79 and 85-86.

Claims 32-38, 41, 44-47, 65-66, 77-78 and 85-86 are rejected under 35 USC 102 (b) as being anticipated by Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS).

Regarding claim 32, Sugii teaches a method comprising:

providing a substrate (p-Si substrate); and

providing a first strained layer (Strained-Si channel layer) disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm, (especially see figs. 1(a)-1(b) and refer to related text, page 2949, last paragraph) .

Regarding claim 33, wherein the substrate comprises Si (p-Si substrate).

Regarding claim 34, wherein the first strained layer comprises Si or Ge (Strained-Si channel layer).

Regarding claim 35, wherein the first strained layer is tensilely strained (comprises Si as claim material).

Regarding claim 36, wherein the first strained layer is compressively strained (comprises Si as claim material).

Regarding claim 37, wherein the first strained layer has a surface roughness of less than approximately 0.77 nm (0.7-0.9 nm, root-mean-square).

Regarding claim 38, further comprising providing an insulator layer disposed beneath the first strained layer.

Regarding claims 41 and 44, further comprising providing a relaxed layer disposed beneath the strained layer and wherein the step of providing a relaxed layer comprises epitaxial growth (Si-Ge buffer layer in fig. 1).

Regarding claims 45- 46, wherein the step or providing a relaxed layer comprises wafer bonding , wherein the relaxed layer comprises SiGe (Si-Ge buffer layer in fig. 1).

Regarding claim 47, wherein the substrate comprises a graded-composition SiGe layer {(GR) buffer layer, especially see fig. 1a and refer to related text}.

Regarding claim 65, wherein the first strained layer has an average surface roughness of less than approximately 0.77 nm (page 2949, "the strained-Si samples are around 0.7-.09 nm and 0.5-0.8 nm).

Regarding claim 66, further comprising providing a gate stack disposed above the first strained layer (gate Al in fig. 1a).

Regarding claims 77- 78, wherein the step of providing the strained layer (Strained-Si channel layer) comprises epitaxial growth and wherein the step of providing the strained layer (Strained-Si channel layer) comprises wafer bonding (especially see figs. 1a-b and refer to related text) .

Regarding claim 85, further comprising providing a relaxed layer (SiGe buffer 1.0 nm layer) disposed beneath the strained layer (Strained-Si); (Especially see figs. 1a-b and refer to related text)

Regarding claim 86, wherein the relaxed layer comprises SiGe (SiGe buffer 1.0 nm layer); (Especially see figs. 1a-b and refer to related text).

Claims 38, 40 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Sugii in view of Mizuno et al. (IEEE ELECTRON DEVICE LETTER Vol. 21. No .5 May 2000/IDS) in view of Mizuno et al. ["Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology", IEEE ELECTRON DEVICE LETTERS, Vol. 21, No. 5, pp. 230-32, May 5, 2000 (Mizuno, hereafter)/IDS]

Regarding claim 38, Sugii teaches the claimed invention as applied to claims 32 and 38 except for the step of providing an insulator layer comprises wafer bonding.

Mizuno discloses "a strained-Si FET structure, MOSFET's on strained-Si/SiGe-on-Insulator (strained-SOD substrates."82 Mizuno states "[t]he strained-SOI structure consists of the strained-Si channel on a relaxed SiGe-on-buried-oxide-layer, as can be seen in the TEM photograph in Fig. 1" (page 230, 2nd column).

Mizuno describes the benefits of incorporating an insulator layer (i.e. the SiO2 layer) in a strained-Si FET, such as the strained-Si FETs described in Sugii "The mobility in strained-Si MOSFET's increases with an increase in strain determined by the Ge content of a SiGe layer beneath strained-Si films. However, the device structure and the fabrication processes of strained-Si MOSFET's have not been necessarily compatible with CMOS standard processes...On the other hand, a SOI structure is another candidate for sub-0.1 devices because the low parasitic capacitance of source/drain junction, high

carrier mobility, simple isolation. In this paper, we propose a new strained-Si FET structure, MOSFET's on strained-Si/SiGe-on-Insulator (strained-SOI) substrates."

Since Sugii discloses strained-Si FET devices, it would have been obvious to one of ordinary skill in the art to combine Sugii with Mizuno to form a FET structure with low parasitic capacitance of source/drain junction, high carrier mobility, and simple isolation.

Regarding claim 40, wherein the step of providing an insulator layer comprises wafer bonding (especially see fig. 1 and refer to related text) .

Claim 53 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Sugii et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) in view of the following remark.

Sugii teaches the claimed invention as applied to claim 32 except for providing a second strained layer disposed above the first strained layer as cited in current claim 53

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a second strained layer disposed above the first strained layer, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Claim 54 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) in view of O'neill et al. (SiGe virtual substrate N-channel heterojunction MOSFETs," Semicond. Sci. Tech., vol. 14, pp. 784-89, 1999/IDS).

Sugii et al. teaches a method comprising:

providing a substrate (p-SI substrate);

providing a first strained layer (Stained–Si channel layer) disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm (the strained –Si samples are around 0.7-0.8 nm and 0.5-0.8 nm, page 2949);

Sugii does not teaches the step of providing a spacer layer disposed above the first strained layer.

O'neill-1999 discloses "[h]eterojunction MOSFETs (HMOSFETs), grown on a virtual substrate of SiGe and having a strained silicon channel. O'Neill-1999 states that "a SiGe barrier layer [is disposed] between the SiO2 layer and the strained Si channel. As shown in Fig. 2 (reproduced below) the SiGe barrier layer is clearly between and separating the "strained-Si" channel layer and the "Si oxide," which is the lower portion of the gate stack. Therefore, O'Neill-1999 discloses a spacer layer between the channel layer and the gate stack. O'Neill-1999 states "[t]he purpose of such a barrier [i.e. spacer layer] is to reduce electron scattering and consequently mobility degradation in the

channel of the HMOSFET. Since Sugii was also directed at "increasing electron mobility in strained-Si MOSFETs, it would have been obvious to one of ordinary skill in the art to combine Sugii with O'Neill-1999 to form a such a MOSFET structure with reduced electron scattering and increased mobility.

Independent claim 39

Claim 39 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Sugii in view of Mizuno et al. (IEEE ELECTRON DEVICE LETTER Vol. 21. No .5 May 2000/IDS).

Sugii teaches the claimed invention as applied to claims 32 and 38 except for the step of providing an insulator layer over the substrate and wherein the insulator layer comprises SiO_2.

Mizuno discloses "a strained-Si FET structure, MOSFET's on strained-Si/SiGe-on-Insulator (strained-SOI substrates). Mizuno states "[t]he strained-SOI structure consists of the strained-Si channel on a relaxed SiGe-on-buried-oxide-layer, as can be seen in the TEM photograph in Fig. 1" (page 230, 2nd column).

Mizuno describes the benefits of incorporating an insulator layer (i.e. the SiO2 layer) in a strained-Si FET, such as the strained-Si FETs described in Sugii "The mobility

in strained-Si MOSFET's increases with an increase in strain determined by the Ge content of a SiGe layer beneath strained-Si films. However, the device structure and the fabrication processes of strained-Si MOSFET's have not been necessarily compatible with CMOS standard processes...On the other hand, a SOI structure is another candidate for sub-0.1 devices because the low parasitic capacitance of source/drain junction, high carrier mobility, simple isolation. In this paper, we propose a new strained-Si FET structure, MOSFET's on strained-Si/SiGe-on-Insulator (strained-SOI) substrates."

Since Sugii discloses strained-Si FET devices, it would have been obvious to one of ordinary skill in the art to combine Sugii with Mizuno to form a FET structure with low parasitic capacitance of source/drain junction, high carrier mobility, and simple isolation.

Set of claims 42-43

Claim 42 is rejected under 35 USC 102 (b) as being anticipated by Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS).

Sugii teaches a method comprising (especially see figs. 1a-b and refer to related text):

providing a substrate (p-Si substrate);

providing a relaxed layer (SiGe buffer layer) over the substrate; and

providing a first strained layer (Strained-Si channel layer) disposed above the substrate and the relaxed layer, the first strained layer (Strained-Si channel layer) having

an average surface roughness of no more than approximately 2 nm, wherein the relaxed layer (SiGe buffer layer) has an average surface roughness of less than approximately 2 nm (the strained –Si samples are around 0.7-0.8 nm and 0.5-0.8 nm).

Claim 43 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) and the following remark.

Sugii et al. teaches the claimed invention as applied to claim 42 except for further comprising planarizing the relaxed layer to reduce surface roughness as cited in current claim 43.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to plannarzing the relaxed layer to reduce surface roughness, because it is commonly used to reduce surface roughness of the relaxed layer, since it has been held to be within the general skill of a worker in the art to select a known process on the basis of its suitability for the desired application.

Independent claim 48

Claim 48 is rejected under 35 USC 102 (b) as being anticipated by Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS).

Sugii et al. teaches a method (especially see figs. 1a-1b, 3 and refer to related text) comprising:

providing a substrate (p-Si substrate);

providing a relaxed layer (SiGe buffer layer) comprising SiGe over the substrate; and

providing a first strained layer (strained-Si channel layer) disposed above the substrate and the relaxed layer, the first strained layer having an average surface roughness of no more than approximately 2 nm (page 2949) , wherein the relaxed layer has an average surface roughness of less than approximately 0.77 nm (the strained –Si samples are around 0.7-0.8 nm and 0.5-0.8 nm, page 2949).

Set of claims 49-52

Claims 49-52 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) and O'neill et al. (SiGe virtual substrate N-channel heterojunction MOSFETs," Semicond. Sci. Tech., vol. 14, pp. 784-89, 1999/IDS).

Regarding claims 49-51, Suggi et al. teaches a method (especially see figs. 1a-b, 3 and refer to related text) comprising:

providing a substrate (p-Si sunbtrate);

providing a relaxed layer (SiGe buffer layer) comprising SiGe over the substrate;

providing a first strained layer (Strained –Si layer) disposed above the substrate and the relaxed layer, the first strained laver having an average surface roughness of no more than approximately 2 nm (the strained –Si samples are around 0.7-0.8 nm and 0.5-0.8 nm, page 2949).

Sugii does not teach step of providing a regrown SiGe layer on the relaxed layer (as cited in claim 49 and give its thickness (wherein the regrown layer has a thickness of less than approximately 2 μm and wherein the regrown layer has a thickness of less than approximately 0.5 μm) as cited in claims 50-51.

O'Neill-1999 teaches a regrown SiGe layer on a relaxed SiGe layer in forming strained channel transistors. O'Neill-1999 states,

The resulting structure [HMOSFET] consisted of the following layers: 1 μm undoped graded-composition buffer, with a linear ramp of Ge content from 0 to 35%, to provide an almost dislocation-free surface on which to grow the device structure; 1 μm relaxed B-doped SiGe (30% Ge) buffer (NA = $1x10^{18}$ cm^{-3}); 10 nm unintentionally doped SiGe spacer; 28 nm unintentionally doped strained Si channel, in which the channel was initially intended to be formed; 5 nm unintentionally doped SiGe (30% Ge), initially intended as a barrier, and finally a 17 nm unintentionally doped Si cap layer ,a proportion of which was consumed during processing. Thus, the electron channel of the HMOSFET

formed at the interface of the gate oxide and the upper strained Si layer. (O'Neill-1999, p. 785, paragraph bridging left and right cols.)

The "10-nm [0.01 μm] unintentionally doped SiGe spacer" reads on the claimed "regrown SiGe layer on the relaxed layer".

O'Neill-1999 fabricated "[h]eterojunction MOSFETs (HMOSFETs), grown on a virtual substrate of SiGe and having a strained silicon channel" [O 'Neill-1999, Abstract, p. 784.] and used computer aided design (TCAD) to determine bulk low field mobility of the strained silicon. [O 'Neill-1999, Abstract, p. 784.] Since Sugii "examined the role of a SiGe buffer layer in increasing electron mobility in strained-Si MOSFETS" [Sugii, p. 2948], it would have been obvious to one of ordinary skill in the art to combine Sugii with O'Neill-1999 to form such a MOSFET structure with increased electron mobility.

Regarding claim 52, wherein the regrown layer is substantially lattice-matched to the relaxed layer (O'Neill-1999, p. 785, paragraph bridging left and right cols.)

Independent claim 55

Claim 55 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) in view of O'neill et al. (SiGe virtual substrate N-channel heterojunction

MOSFETs," Semicond. Sci. Tech., vol. 14, pp. 784-89, 1999/IDS) and further in view of O'Neill et al.(Deep Submicron CMOS Based on Silicon Germanium Technology, IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 43, No. 6, June, 1996).

Sugii et al. teaches a method comprising:

providing a substrate (p-SI substrate);

providing a first strained layer (Stained–Si channel layer) disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm (the strained –Si samples are around 0.7-0.8 nm and 0.5-0.8 nm, page 2949);

Sugii does not teaches the step of providing a spacer layer disposed above the first strained layer, wherein the spacer layer has a thickness of less than approximately 5 nm.

O'neill-1999 discloses "[h]eterojunction MOSFETs (HMOSFETs), grown on a virtual substrate of SiGe and having a strained silicon channel. O'Neill-1999 states that "a SiGe barrier layer [is disposed] between the SiO2 layer and the strained Si channel. As shown in Fig. 2 (reproduced below) the SiGe barrier layer is clearly between and separating the "strained-Si" channel layer and the "Si oxide," which is the lower portion of the gate stack. Therefore, O'Neill-1999 discloses a spacer layer between the channel layer and the gate stack. O'Neill-1999 states "[t]he purpose of such a barrier [i.e. spacer layer] is to reduce electron scattering and consequently mobility degradation in the channel of the HMOSFET. Since Sugii was also directed at "increasing electron mobility

in strained-Si MOSFETs, it would have been obvious to one of ordinary skill in the art to combine Sugii with O'Neill-1999 to form a such a MOSFET structure with reduced electron scattering and increased mobility.

In view of Sugii with O'Neill-1999 does not teach the spacer layer has a thickness of less than approximately 5 nm.

O'Neill-1996 teaches the spacer layer has a thickness of less than approximately 5 nm.

O'Neill-1996 discloses "both n-and p-channel FET's grown on a relaxed Si 0.7Ge 0.3 buffer. The n-channel device geometry for the heterojunction MOS-FET's (HNMOSFET's) under consideration here is shown in Fig. 1 (a) . "The device consists of a strained Si channel, of thickness 10 nm grown on a relaxed Si 0.7Ge 0.3 buffer. Above the Si channel is a Si 0.7Ge 0.3 cap layer of variable thickness and above that an oxide of thickness 5 nm. As shown in Fig. 1(a) (reproduced below) the Si 0.7Ge 0.3 cap layer of variable thickness is clearly between and separating the "Si channel" layer and the "oxide," which is the lower portion of the gate stack.

Therefore, the O'Neill 1996 n-channel device discloses a spacer layer between the channel layer and the gate stack."The p-channel device (HPMOSFET) is shown in Fig. 1 (b). Like the n-channel device, it is grown on a relaxed Si 0.7Ge 0.3 buffer layer. The channel for the HPMOSFET is a 10-nm thick Si 0.7Ge 0.3 layer and the cap layer is Si. As shown in Fig. 1(b) (reproduced below) the Si cap layer is clearly between and

separating the " Si 0.7Ge 0.3 channel" layer and the "oxide," which is the lower portion of the gate stack. Therefore, the O'Neill-1996 p-channel device discloses a spacer layer between the channel layer and the gate stack.

O'Neill-1996 states this structure improves channel mobility "which derives in part from the higher bulk mobility seen in strained Si and in part because channel electrons in the HMOSFET devices do not experience the transverse field dependent mobility reductions found in conventional surface channel operation. Since Sugii was also directed at "increasing electron mobility in strained-Si MOSFETs, it would have been obvious to one of ordinary skill in the art to combine Sugii with O'Neill-1996 to form a such a MOSFET structure with increased mobility.

Independent claim 56

Claim 56 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) in view of O'Neill et al.(Deep Submicron CMOS Based on Silicon Germanium Technology, IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 43, No. 6, June, 1996).

Sugii et al. a method comprising:

providing a substrate (p-Si sunstrate);

providing a first strained layer (Strained-Si channel layer) disposed above the

substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm {Sugii discloses a strained-Si channel layer where the measured surface roughness "of the strained-Si samples are around 0.7-0.9 nm [root-mean-square] and 0.5-0.8 nm [average roughness curvature]" (Sugii p.2949)}; and

Sugii does not teach providing a spacer layer disposed above the first strained layer, wherein the first strained layer comprises Ge and the spacer layer consists essentially of Si as cited in current claim.

O'neill-1996 teaches a spacer layer disposed above the first strained layer, wherein the first strained layer comprises Ge and the spacer layer consists essentially of Si [0 'Neill-1996 describes the p-channel device in Fig. l(b) where "[t]he channel for the HPMOSFET is a 10-nm thick $Si_{0.7}Ge_{0.3}$ layer and the cap layer is Si." (O "Neill 1996 p.912).Hence, the Si cap layer p-channel device operates as a "'spacer layer'" as used in the current claim. Accordingly, 0'Neill-1996 discloses a $Si_{0.7}Ge_{0.3}$ channel layer that comprises Ge, and a Si cap (spacer) layer consisting essentially of Si.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a spacer layer disposed above the first strained layer, wherein the first strained layer comprises Ge and the spacer layer consists essentially of Si in Sugii 's method in order to form a such a MOSFET structure with increased mobility.

Set of claims 57-58

Claims 57-58 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) in view of O'Neill et al.(Deep Submicron CMOS Based on Silicon Germanium Technology, IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 43, No. 6, June, 1996) and further in view of the following remark.

Sugii teaches a method comprising:

providing a substrate (p-Si substrate);

providing a first strained layer disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm {Sugii discloses a strained-Si channel layer where the measured surface roughness "of the strained-Si samples are around 0.7-0.9 nm [root-mean-square] and 0.5-0.8 nm [average roughness curvature]" (Sugii p.2949)};

Sugii does not teach providing a spacer layer disposed above the first strained layer; and providing a second strained layer disposed above the spacer layer.

O'neill-1996 teach a spacer layer disposed above the first strained layer, wherein the first strained layer comprises Ge and the spacer layer consists essentially of Si [0 'Neill-1996 describes the p-channel device in Fig. l(b) where "[t]he channel for the HPMOSFET is a 10-nm thick $Si_{0.7}Ge_{0.3}$ layer and the cap layer is Si." (O "Neill 1996

p.912).Hence, the Si cap layer p-channel device operates as a "'spacer layer'" as used in the current claim. Accordingly, 0'Neill-1996 discloses a $Si_{0.7}Ge_{0.3}$ channel layer that comprises Ge, and a Si cap (spacer) layer consisting essentially of Si.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a spacer layer disposed above the first strained layer, wherein the first strained layer and the spacer layer in Sugii 's method in order to form a such a MOSFET structure with increased mobility.

Sugii in view of O'neill-1966 does not teach a second strained layer disposed above the first strained layer as cited in current claim.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a second strained layer disposed above the first strained layer, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Regarding claim 58, further comprising providing a gate stack disposed above the second strained layer (Sugii, fig. 1a).

Independent claim 59

Claim 59 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS)

in view of O'neill et al. (SiGe virtual substrate N-channel heterojunction MOSFETs," Semicond. Sci. Tech., vol. 14, pp. 784-89, 1999/IDS).

Sugii et al. teaches a method comprising:

providing a substrate (p-SI substrate);

providing a first strained layer (Stained–Si channel layer) disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm {Sugii discloses a strained-Si channel layer where the measured surface roughness "of the strained-Si samples are around 0.7-0.9 nm [root-mean-square] and 0.5-0.8 nm [average roughness curvature]" (Sugii p.2949).

Sugii does not teach providing a spacer layer disposed above the first strained layer, wherein the spacer layer comprises Ge as cited in current claim.

O'neill-1999 discloses "[h]eterojunction MOSFETs (HMOSFETs), grown on a virtual substrate of SiGe and having a strained silicon channel. O'Neill-1999 states that "a SiGe barrier layer [is disposed] between the SiO2 layer and the strained Si channel. As shown in Fig. 2 (reproduced below) the SiGe barrier layer is clearly between and separating the "strained-Si" channel layer and the "Si oxide," which is the lower portion of the gate stack. Therefore, O'Neill-1999 discloses a spacer layer between the channel layer and the gate stack. O'Neill-1999 states "[t]he purpose of such a barrier [i.e. spacer layer] is to reduce electron scattering and consequently mobility degradation in the

channel of the HMOSFET. Since Sugii was also directed at "increasing electron mobility in strained-Si MOSFETs, it would have been obvious to one of ordinary skill in the art to combine Sugii with O'Neill-1999 to form a such a MOSFET structure with reduced electron scattering and increased mobility.

Set of claims 60-64.

Claims 60, 61-63 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) in view of O'neill et al. (SiGe virtual substrate N-channel heterojunction MOSFETs," Semicond. Sci. Tech., vol. 14, pp. 784-89, 1999/IDS).

Sugii et al. teaches a method comprising:

providing a substrate (p-SI substrate);

providing a first strained layer (Stained–Si channel layer) disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm {Sugii discloses a strained-Si channel layer where the measured surface roughness "of the strained-Si samples are around 0.7-0.9 nm [root-mean-square] and 0.5-0.8 nm [average roughness curvature]" (Sugii p.2949).

Sugii does not teach providing a spacer layer disposed above the first strained layer; and providing a gate stack disposed above the spacer layer as cited in current claim.

O'neill-1999 discloses "[h]eterojunction MOSFETs (HMOSFETs), grown on a virtual substrate of SiGe and having a strained silicon channel. O'Neill-1999 states that "a SiGe barrier layer [is disposed] between the SiO2 layer and the strained Si channel. As shown in Fig. 2 (reproduced below) the SiGe barrier layer is clearly between and separating the "strained-Si" channel layer and the "Si oxide," which is the lower portion of the gate stack. Therefore, O'Neill-1999 discloses *a spacer layer between the channel layer and the gate stack.* O'Neill-1999 states "[t]he purpose of such a barrier [i.e. spacer layer] is to reduce electron scattering and consequently mobility degradation in the channel of the HMOSFET. Since Sugii was also directed at "increasing electron mobility in strained-Si MOSFETs, it would have been obvious to one of ordinary skill in the art to combine Sugii with O'Neill-1999 to form a such a MOSFET structure with reduced electron scattering and increased mobility.

Regarding claims 61 and 63, further comprising providing supply layer dopants located in the spacer layer and further comprising providing supply layer dopants located below the strained layer {O'Neill 1999 describes device fabrication of the HMOSFET structure as comprising the following layers:

"1 μm undoped graded-composition buffer, with a linear ramp of Ge content

from 0 to 35%, to provide an almost dislocation-free surface on which to grown the device structure; 1 lam relaxed B-doped SiGe (30% Ge) buffer (NA = 1 x 10is cm" 3); 10 nm unintentionally doped Si(3e spacer; 28 nm unintentionally doped strained Si channel, in which the channel was initially intended to be formed; 5 nm unintentionally doped SiGe (30% Ge), initially intended as a barrier, and finally a 17 nm unintentionally doped Si cap layer." (O'Neill 1999p.785). The "relaxed B-doped SiGe (30% Ge) buffer (NA = 1 x 1018 cm-3) "' layer is a portion of the virtual substrate which lies below the strained-Si channel layer.}.

Regarding claims 62 and 64, Sugii in view of Oneill-1999 teaches the claimed invention as applied to claims 60, 61 and 63 except for wherein the supply layer dopants are provided by implantation as cited in current claims 62 and 64.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize implantation process to form the supply layer, because it is commonly used to obtain the best resultant doped regions, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the practical application.

Set of claims 67-69

Claim 67 is rejected under 35 USC 102 (b) as being anticipated by Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS).

Sugii teaches a method comprising:

providing a substrate (p-Si substrate);

providing a first strained layer (Strained-Si channel layer) disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm {Sugii discloses a strained-Si channel layer where the measured surface roughness "of the strained-Si samples are around 0.7-0.9 nm [root-mean-square] and 0.5-0.8 nm [average roughness curvature]" (Sugii p.2949)};

providing a gate stack (Gate Al) disposed above the first strained layer; and

providing device isolation regions (especially see figs. 1a-b, 3 and refer to related text) .

Regarding claim 68 and 69, wherein the device isolation regions are STI regions and wherein the device isolation regions are LOCOS regions (especially see figs. 1a-b and refer to related text).

Set of claims 70-76

Claim 70 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) in view of the following remark.

Sugii teaches a method (especially see figs. 1a-b and refer to related text) comprising:

providing a substrate (p-Si substrate);

providing a first strained layer (strained-Si channel layer) disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm {Sugii discloses a strained-Si channel layer where the measured surface roughness "of the strained-Si samples are around 0.7-0.9 nm [root-mean-square] and 0.5-0.8 nm [average roughness curvature]" (Sugii p.2949)};

providing a gate stack (Gate Al) disposed above the first strained layer;

Sugii does not teach the step of providing metal silicide regions.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide metal silicide regions in Sugii 's method in order to enhance conductivities to surrounding regions.

Regarding claims 71-76, Reasons for Indication of Allowable Subject Matter.

Reasons for Indication of Allowable Subject Matter.

Claims 71-76 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered

pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) in view of O'neill et al. (SiGe virtual substrate N-channel heterojunction MOSFETs," Semicond. Sci. Tech., vol. 14, pp. 784-89, 1999/IDS) and further in view of O'Neill et al.(Deep Submicron CMOS Based on Silicon Germanium Technology, IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 43, No. 6, June, 1996), taken individually or in combination, do not teach the claimed invention having **(Regarding claim 71)** the metal silicide regions comprise alloyed metal-SiGe **(Regarding claim 72)** the metal is selected from the group consisting of: Ti, Co, and Ni. **(Regarding claim 73)** the step of providing metal silicide regions comprises deposition followed by annealing, **(Regarding claim 74)** providing source and drain contact areas, **(Regarding claim 75)** providing an additional SiGe or Ge layer in the source and drain contact areas prior to providing metal silicide regions and **(Regarding claim 76)** providing an additional Si layer above the SiGe or Ge layer prior to providing metal silicide regions.

Set of claims 80-84, 87-88 are allowed.

The following is a statement of reason for the indication of allowable subject matter:

Claims 80-84, 87-88 are considered allowable since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Suggi et al. (Applied Physics Letters, Vol. 75, No. 19, pp. 2948-50, November 8, 1999/IDS) in view of O'neill et al. (SiGe virtual substrate N-channel heterojunction MOSFETs," Semicond. Sci. Tech., vol. 14, pp. 784-89, 1999/IDS) and further in view of O'Neill et al.(Deep Submicron CMOS Based on Silicon Germanium Technology, IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 43, No. 6, June, 1996), taken individually or in combination, do not teach the claimed invention having **(Regarding claim 80)** step of providing metal silicide regions: wherein the first strained layer has an average surface roughness of less than approximately 0.77 nm.

If Applicants are aware of better art than that which has been cited, they are required to call such to attention of the examiner.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, M. Smith can be reached on (571) 272-1907. The central fax phone numbers for the organization where this application or proceeding is assigned are (571)272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
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